

We claim:

- 1 1. A mixed analog/digital integrated circuit comprising:
 - 2 (a) a silicon substrate having a surface,
 - 3 (b) a digital device section in the substrate, the digital device section
 - 4 comprising an array of MOS transistors operating at a voltage V_D that
 - 5 steps from a first value V_{D1} to a second value V_{D2} ,
 - 6 (c) a p-n junction guard ring surrounding the digital device section, the
 - 7 guard ring comprising impurity regions extending from the surface of the
 - 8 substrate to a depth of at least d below the surface of the substrate,
 - 9 (d) an analog device section in the substrate spaced laterally from the
 - 10 digital device section, the analog device section comprising an array of
 - 11 MOS transistors operating with a voltage V_A that varies continuously
 - 12 from V_{A1} to V_{A2} ,
 - 13 (e) a triple well isolation region comprising a doped layer that extends
 - 14 beneath the digital device region at a depth d and contacts the p-n
 - 15 junction guard ring,
 - 16 and wherein the analog device section is devoid of triple well isolation
 - 17 region.
- 1 2. The integrated circuit of claim 1 wherein the array of MOS transistors in the
- 2 digital device section comprise pairs of CMOS transistors.

1 3. The integrated circuit of claim 2 wherein the array of MOS transistors in the
2 analog device section comprise pairs of CMOS transistors.

1 4. The integrated circuit of claim 1 wherein d is in the range 2 - 10 microns.

1 5. An integrated circuit formed in a p-type silicon substrate and comprising:

2 (a) a digital device section, the digital device section having a first region,
3 a second region and a third region and comprising:

4 (i) an n-well formed in the first region of the digital device section,

5 (ii) at least one p-channel transistor formed in the first n-well,

6 (iii) means for applying to the p-channel transistor a voltage V_D that
7 steps from a first value, V_{D1} , to a second value, V_{D2} ,

8 (iv) at least one n-channel transistor formed in the second region of
9 the digital device section,

10 (v) means for applying to the n-channel transistor a voltage V_D that
11 steps from a first value, V_{D1} , to a second value, V_{D2} ,

12 (vi) at least one n-well resistor formed in the third region of the
13 digital device section,

14 (b) an analog device section, the analog section comprising a first region,
15 and a second region, and comprising:

16 (i) an n-well formed in the first region of the analog device section,

17 (ii) at least one p-channel transistor formed in the first n-well,

(iii) means for applying to the p-channel transistor a voltage V_A that varies over a range of voltages between a first value, V_{A1} , and a second value, V_{A2} ,

(iv) at least one n-channel transistor formed in the second region of the analog device section,

(v) means for applying to the n-channel transistor a voltage V_A that varies over a range of values between a first value, V_{A1} , and a second value, V_{A2} ,

(c) means for connecting the first and second regions of the digital device section to digital V_{SS} ,

(d) means for connecting the first and second regions of the analog device section, and the third region of the digital device section to analog V_{SS} ,

(e) a first n-type guard ring surrounding the first, second, and third regions of the digital device section, the first n-type guard ring extending from the surface of the substrate to a depth of at least d below the surface of the substrate,

(f) a second n-type guard ring surrounding the third region of the digital device section, the second n-type guard ring situated within, and spaced from, the first n-type guard ring and extending from the surface of the substrate to a depth of at least d below the surface of the substrate,

(g) an n-type triple well isolation region selectively formed at a depth d underneath said first and second regions of the digital device section and

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joined to the first and second n-type guard rings.

1 6. The integrated circuit of claim 5 wherein d is in the range 2 - 10 microns.

1 7. An integrated circuit formed in an n-type silicon substrate and comprising:

2 (a) a digital device section, the digital device section having a first region,
3 a second region and a third region and comprising:

4 (i) a p-well formed in the first region of the digital device section,

5 (ii) at least one n-channel transistor formed in the first p-well,

6 (iii) means for applying to the n-channel transistor a voltage V_D that
7 steps from a first value, V_{D1} , to a second value, V_{D2} ,

8 (iv) at least one p-channel transistor formed in the second region of
9 the digital device section,

10 (v) means for applying to the p-channel transistor a voltage V_D that
11 steps from a first value, V_{D1} , to a second value, V_{D2} ,

12 (vi) at least one p-well resistor formed in the third region of the
13 digital device section,

14 (b) an analog device section, the analog section comprising a first region,
15 and a second region, and comprising:

16 (i) a p-well formed in the first region of the analog device section,

17 (ii) at least one n-channel transistor formed in the first p-well,

18 (iii) means for applying to the n-channel transistor a voltage V_A that

varies over a range of voltages between a first value, V_{A1} , and a second value, V_{A2} ,

(iv) at least one p-channel transistor formed in the second region of the analog device section,

(v) means for applying to the p-channel transistor a voltage V_A that varies over a range of values between a first value, V_{A1} , and a second value, V_{A2} ,

(c) means for connecting the first and second regions of the digital device section to digital V_{DD} ,

(d) means for connecting the first and second regions of the analog device section, and the third region of the digital device section to analog V_{DD} ,

(e) a first p-type guard ring surrounding the first, second, and third regions of the digital device section, the first p-type guard ring extending from the surface of the substrate to a depth of at least d below the surface of the substrate,

(f) a second p-type guard ring surrounding the third region of the digital device section, the second p-type guard ring situated within, and spaced from, the first p-type guard ring and extending from the surface of the substrate to a depth of at least d below the surface of the substrate,

(g) a p-type triple well isolation region selectively formed at a depth d underneath said first and second regions of the digital device section and joined to the first and second p-type guard rings.